Novel Through-Silicon Via Technologies for 3D System Integration

Paragkumar A. Thadesar, Ashish Dembla, Devin Brown and Muhannad S. Bakir

School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, USA
pthadesar3@gatech.edu and muhannad.bakir@mirc.gatech.edu

ABSTRACT

To circumvent the performance and energy bottlenecks due to interconnects, novel interconnect solutions are needed both at the package and die levels. This paper reports (1) novel photodefined polymer-embedded vias within silicon interposers for improved through-silicon via insertion loss, and (2) ultrahigh density low-capacitance nanoscale TSVs with 100 nm diameter and 20:1 aspect ratio for fine-grain 3D IC implementation.

INTRODUCTION

System-level interconnection has emerged as a critical bottleneck to achieving faster and lower-power systems and thus creating a need for innovative solutions. However, there is no single innovative technology, i.e., 'silver bullet,' that will address the performance, energy dissipation, scalability, and ability to integrate heterogeneous components (logic, memory, sensors, photonics, and RF functionality) of future electronic systems. The interconnect problem is very multiscale in nature covering a wide range of interconnect dimensions and distances (nanometers to meters; on- vs. off-chip). Disruptive architectural innovations will result by exploiting novel technological advances in signaling at all length scales, which is the key to this research. Packaging advances involving 2.5-dimensional (2.5D) interposer technology have occurred in parallel to advances in 3-dimensional (3D) IC integration using through-silicon vias (TSVs) and are widely explored in the literature [1, 2]. However, TSV requirements differ at the silicon interposer and 3D IC levels.

With respect to silicon interposers, large area interposers can support a larger number of chips yielding increased system functionality. Increasing the thickness of a silicon interposer alleviates concerns over the warpage profile of large area interposers, but it also increases TSV length, leading to increased TSV RF losses [3, 4]. High resistivity silicon can be used to reduce TSV losses but is expensive [5]. Moreover, TSV losses can be reduced by increasing the thickness of the dielectric liner [6, 7]. However, even greater reduction in TSV losses can be obtained by implementing a substrate other than silicon (for example, glass) [8, 9]. But the fabrication of through-glass vias is still evolving.

With respect to 3D ICs, although TSVs are able to provide reduced wire lengths, they consume silicon real estate. For example, a single 5 µm diameter TSV consumes ~218 times the area required for a 0.09 μm^2 6T SRAM cell in IBM 22 nm technology [10] without accounting for keep-away zones. Further scaling of TSV diameter can significantly save silicon real estate. M. Koyonagi et al. [11] have demonstrated 700 nm diameter and 18 µm tall TSVs using W/poly-Si. J. Knickerbocker et al. [2] have shown 140 nm diameter TSVs in thin layers. Moreover, TSVs can be used as deep trench decoupling capacitors [12]. However, experimental fabrication of highly-scaled high aspect ratio nanoscale TSVs has not been demonstrated.

Hence, different innovative interconnection solutions are required across the system-level hierarchy and to address this demand, two novel TSV technologies are demonstrated in this paper: 1) polymer-embedded vias within silicon interposers for reduced TSV RF losses, and 2) nanoscale TSVs for 3D ICs to obtain ultrahigh TSV density with reduced TSV capacitance and to enable fine-grain 3D IC implementation [13, 14]. Fig. 1 shows a schematic of a silicon interposer with polymer-embedded vias, supporting 3D ICs with nanoscale TSVs.

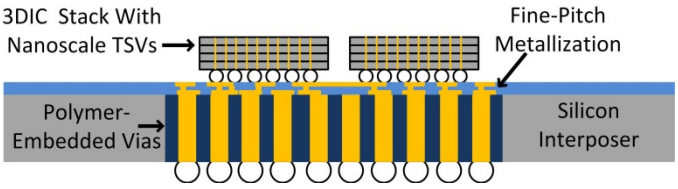

Fig. 1. Silicon interposer with polymer-embedded vias and 3D ICs consisting of ultra-dense nanoscale TSVs mounted atop the interposer

POLYMER-EMBEDDED VIAS

Polymer-embedded vias are fabricated by embedding copper vias within photodefined polymer wells in a low-resistivity silicon interposer. The fabrication of polymer-embedded vias begins by depositing silicon dioxide, titanium and copper on a silicon wafer, as shown in Fig. 2.

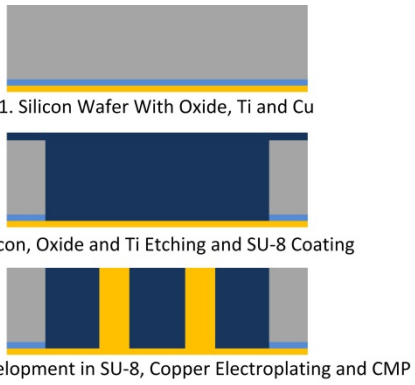

Fig. 2. Fabrication process for polymer-embedded vias

Next, wells are etched in silicon followed by the etching of silicon dioxide and titanium at the bottom of the wells. Following the etching, SU-8 is spin coated and soft baked. Next, the polymer-filled well is UV exposed to pattern vias within the polymer well [15]. Post exposure bake is performed next followed by development in SU-8 developer and

978-1-4799-0440-2/13/$31.00 © 2013IEEE

isopropanol clean to yield vias in the SU-8-filled wells. Next, bottom up copper electroplating is performed using a copper electroplating solution from Enthone, followed by chemical mechanical polishing (CMP) using a slurry from Cabot Microelectronics Corporation to remove overburden copper resulting in polymer-embedded vias. Using this fabrication flow, polymer-embedded vias were fabricated with different diameters. In Fig. 3, 270 µm tall and 100 µm diameter copper vias on a 250 µm pitch are embedded within 1000 µm x 1000 µm polymer-filled wells in silicon. To confirm the high yield of the fabricated polymer-embedded vias, 4-point resistance measurements were performed, yielding 2.54 mΩ average measured resistance for 20 vias.

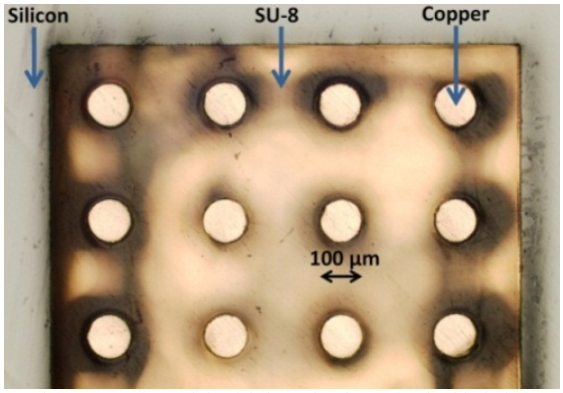

Fig. 3. Top view of the fabricated polymer-embedded vias

Since a dielectric is present between the copper vias, instead of silicon and silicon dioxide as in conventional TSVs, a significant reduction in TSV insertion loss can be expected compared to the conventional TSVs [8, 9]. To characterize the high-frequency behavior of polymer-embedded vias, RF measurements were performed from 100 MHz to 50 GHz using a dedicated RF probe station with Agilent N5245A PNA-X network analyzer and Cascade |Z| Probes (Fig. 4). Prior to the measurements of TSVs, calibration of the probes was performed using LRRM calibration protocol, de-embedding the TSV RF measurements. Next, RF measurements were performed for polymer-embedded vias with GSG TSV structure as shown in Fig. 4.

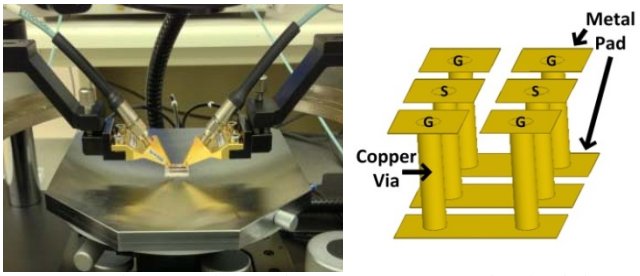

Fig. 4. RF probe setup (left) and GSG TSV structure for simulations and measurements of polymer-embedded vias (right)

To verify the measurements, full-wave electromagnetic simulations were performed in Ansoft High-Frequency Structure Simulator (HFSS) from 100 MHz to 50 GHz with 3.25 and 0.035 as the relative dielectric constant and the loss tangent of SU-8, respectively [16]. The measured insertion loss (S21) was approximately 1 dB at 50 GHz as demonstrated in Fig. 5.

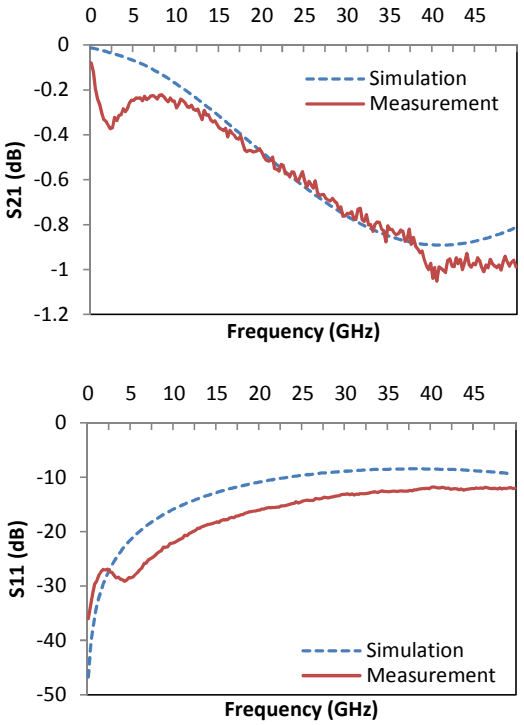

Fig. 5. High-frequency simulation and measurement results for polymer-embedded vias with via-trace-via structure

NANOSCALE TSVS

Ultrahigh density TSVs are fabricated by scaling TSV diameter to 100 nm while simultaneously increasing TSV aspect ratio to 20:1. Nanoscale TSVs are dimensionally comparable to on-chip local metal interconnects and offer ultrahigh density vertical interconnection (>10^8/cm^2). At 100 nm diameter, it is possible to place ~127 million TSVs in 1% area of a 1 cm^2 die. The reduced TSV footprint provides a pathway to reduce capacitance of vertical interconnects and to allow fine-grain 3D IC implementation, which in turn helps reduce system-level power dissipation and improve performance. Using the TSV dielectric capacitance model from [17], Fig. 6 shows the reduction in TSV dielectric capacitance that can be obtained by scaling the TSV dimensions. Assuming TSV dielectric (silicon dioxide with 3.9 relative dielectric constant) thickness equal to 20% of the TSV outer diameter and assuming TSV aspect ratio as 20:1, TSV dielectric capacitance is 42.5 fF and 0.849 fF (50X reduction), respectively, for TSVs with 5 µm and 100 nm diameter, respectively.

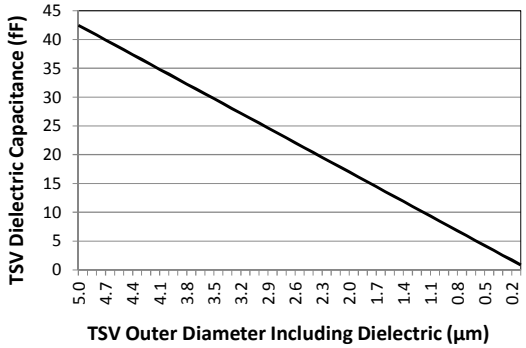

Fig. 6. TSV dielectric capacitance as a function of TSV outer diameter

Nanoscale TSVs are fabricated in a 2 µm thick device layer of a custom SOI wafer with 1.5 µm buried oxide and 300 µm thick handle. As shown in Fig. 7, the fabrication of nanoscale TSVs begins with electron beam lithography on the device side of an SOI wafer using JEOL JBX 9300FS at 100kV acceleration voltage, 2 nA beam current and a shot pitch of 6 nm. Positive tone electron beam resist ZEP520A was used as an etch mask for silicon Bosch process etching. Exposed resist was developed using a 2 minute Amyl-Acetate immersion at room temperature yielding the pattern shown in Fig. 8. Next, nanoscale vias are etched using Bosch process and the buried oxide is used as an etch stop layer. TSV etching was performed on different geometries to estimate taper in blind vias, as shown in Fig. 9(a). The etch depth of these TSVs is limited by the mask thickness and mask etch selectivity [18].

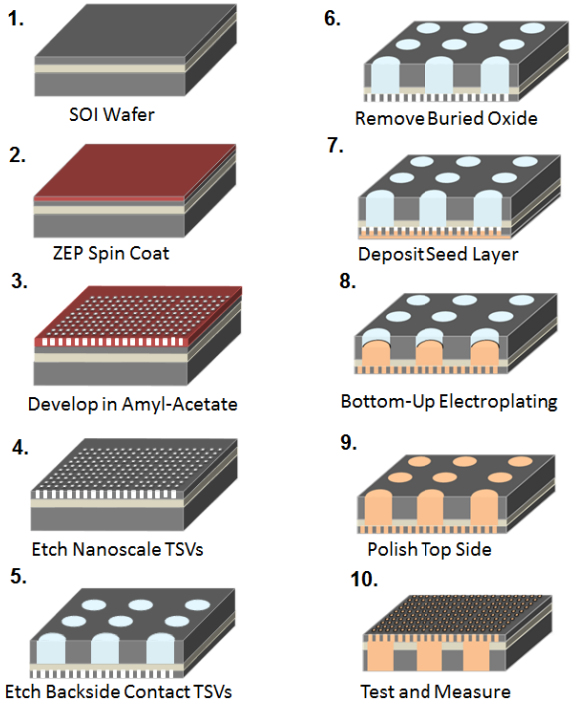

Fig. 7. Fabrication process for nanoscale TSVs

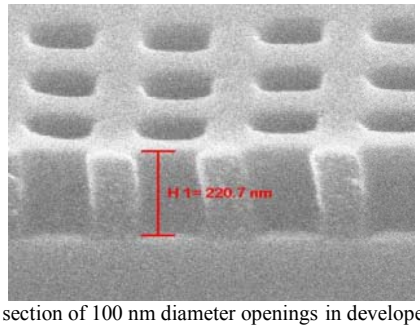

Fig. 8. Cross section of 100 nm diameter openings in developed photoresist

In order to perform bottom up electroplating of vias, a seed layer needs to be deposited on one end of the through vias. Bottom contacts are etched in the handle layer of the SOI wafer to remove silicon all the way to the buried oxide layer. Buffered hydrofluoric acid (5:1 BHF) is used to remove the buried oxide layer. After complete removal of the BOX layer, thermal oxidation is performed to grow a thin oxide (~20 nm) followed by deposition of a thin seed layer of Ti/Cu/Ti on the device layer of the SOI wafer. Due to the small dimensions, nanoscale TSVs act as super fine mesh [19] that achieves closure for the deposited seed layer. Next, bottom up copper electroplating is performed yielding copper plated nanoscale TSVs. Fig. 9 shows the fabricated nanoscale TSVs with ~100 nm diameter and ~20:1 aspect ratio.

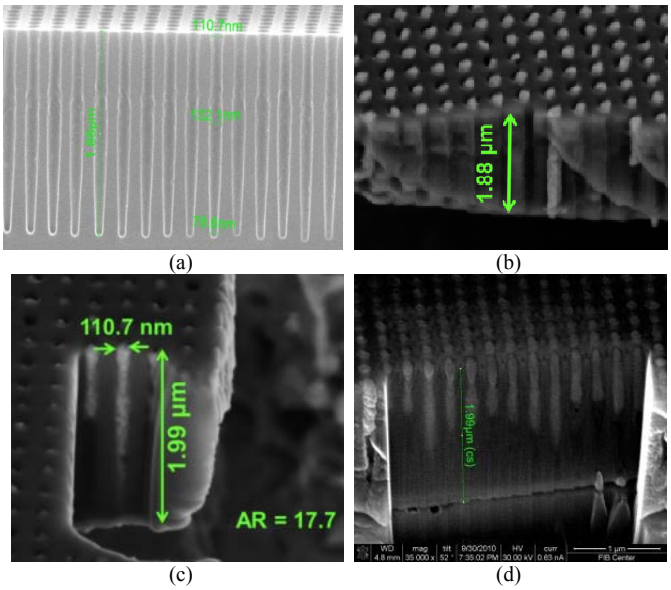

Fig. 9. Fabricated nanoscale TSVs (a) blind ~100 nm diameter vias, (b) and (c) cross section of fully plated TSVs, and (d) cross section with copper removed near via bottom during focused ion beam (FIB) cross sectioning

CONCLUSION

To address future interconnection challenges, low-loss photodefined polymer-embedded vias were demonstrated for silicon interposers, and ultrahigh density nanoscale TSVs were demonstrated for 3D ICs. Further scaling of polymer-embedded vias and characterization of the nanoscale TSVs is work in progress.

ACKNOWLEDGEMENT

The authors gratefully acknowledge support from Semiconductor Research Corporation (SRC) [Contract numbers 2012-KJ-2256 and 2012-KJ-2254].

REFERENCES

[1] J. U. Knickerbocker et al., *ECTC*, 2012.
[2] J. U. Knickerbocker et al., *IBM J. Res. Dev.*, 2008.
[3] M. Sunohara et al., *ECTC*, 2010.
[4] J. S. Pak et al., *EMAP*, 2007.
[5] B. Xie et al., *EMC*, 2011.
[6] Y.-J. Chang et al., *ECTC*, 2012.
[7] M. Parekh et al., *ECTC*, 2011.
[8] I. Ndip et al., *IEEE Tran. Comp. Pack. Man. Tech.*, 2011.
[9] T. Bandyopadhyay et al., *3DIC*, 2009.
[10] B. S. Haran et al., *IEDM*, 2008.
[11] M. Koyonagi et al., *Proc. IEEE*, 2009.
[12] B. Dang et al., *IEEE EDL*, 2010.
[13] D. Sekar, *Invited Talk, IEEE CPMT Soc.*, 2012.
[14] Y.-J. Lee et al., *ICCAD*, 2012
[15] P. Thadesar et al., *J. Micromech. Microeng.*, 2013.
[16] S. W. Ho et al., *ECTC*, 2008.
[17] G. Katti et al., *IEEE Tran. Elec. Dev.*, 2010.
[18] B. Wu et al., *J. Appl. Phy.*, 2010.
[19] J.-H. Lai et al., *J. Micromech. Microeng.*, 2010.